REMARKS

Claims 1, 6-8, 10, and 15-20 are currently pending in this application.

In the last Office Action, the Examiner objected to the drawings and stated that "a first wiring comprising one end positioned in said first pad and **comprising the other end positioned in the peripheral portion of the inner region of the chip**, and a second wiring comprising one end positioned in the second pad **and comprising the other end positioned in the peripheral portion of the inner region of the chip** must be shown or the feature(s) canceled from the claim(s)." Office Action, pg. 2 (emphasis in original).

The Examiner rejected claims 1, 6-8, 10, and 15-20 under 35 U.S.C. § 112, second paragraph, "as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." Office Action, pg. 3. The Examiner also rejected claims 1, 6-8, 10, and 15-20 under 35 U.S.C. § 103(a) as being unpatentable over so-called admitted prior art and in view of U.S. Patent No. 5,679,967 to Janai et al. (hereinafter, "Janai"). Office Action, pp. 3-4.

Applicants respectfully traverse these objections and rejections for the following reasons.

OBJECTION TO DRAWINGS UNDER 37 C.F.R. § 1.83(a)

The Examiner states that "a first wiring comprising one end positioned in said first pad and **comprising the other end positioned in the peripheral portion of the inner region of the chip**, and a second wiring comprising one end positioned in the second pad **and comprising the other end positioned in the peripheral portion of the inner**

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region of the chip must be shown or the feature(s) canceled from the claim(s)." Office Action, pg. 2 (emphasis in original). Applicants have amended claim 1 to more appropriately define the present invention. In addition, Applicants respectfully direct the Examiner to the exemplary embodiment depicted in Fig. 1 in which all features contained within claim 1 are shown. Specifically, Applicants direct the Examiner to wirings 14 and 17 which each have one end positioned at a "peripheral portion of the inner region of the chip," as indicated by the line separating the "Chip Inner Area" and the "Chip Outermost Area Peripheral Area." Accordingly, Applicants respectfully submit that the drawings support these claimed features and request the Examiner to withdraw the objection to the drawings.

In making the various references to the drawings set forth herein, it is to be understood that Applicants are in no way intending to limit the scope of the claims to the exemplary embodiments shown in the drawings and described in the specification. Rather, Applicants expressly affirm that they are entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law.

REJECTION UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

The Examiner states that "[i]t is unclear how a first wiring **comprises the other end positioned in the peripheral portion of the inner region of the chip**, and a second wiring **comprises the other end positioned in the peripheral portion of the inner region of the chip**." Office Action, pg. 3 (emphasis in original). Applicants have amended claim 1 to more appropriately define the present invention and accordingly,

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respectfully request the Examiner to withdraw this basis for rejection of claims 1, 6-8, 10, and 15-20 under 35 U.S.C. § 112, second paragraph.

The Examiner further stated that the recitation "a first pad arranged on a wiring level different from said first I/O slot and arranged above the first I/O slot **without being connected to the first I/O slot**" was unclear. Office Action, pg. 3 (emphasis in original). The Examiner further alleged that "[i]n Fig. 1, it appears that the first pad 12a is part of first I/O slot 11a and is therefore 'connected' to the first I/O slot." *Id.*

However, Fig. 1 is "a plan view showing a semiconductor integrated circuit device according to one embodiment of the present invention." Application, pg. 6, ll. 21-23. Because it is a figure in a plan view, Applicants respectfully direct the Examiner to Fig. 2 which is "an oblique view showing the rewiring of the chip outermost area peripheral area." Application, pg. 6, ll. 24-25. Although, according to the Examiner, in Fig. 1, "it appears that the first pad 12a is part of first I/O slot 11a and is therefore 'connected' to the first I/O slot," Fig. 2, which illustrates a slanted angle and illustrates the relationships between the different levels, shows pad 12a above slot 11a and not having any connection to slot 11a. First pad 12a is not arranged on the same wiring level as the first I/O slot 11a and is not part of the first I/O slot 11a. Specifically, pad 12a connects to via 15 (through wiring 14) and further connects to via 22 (through wiring 21). Via 22 is connected to via 23 and, through wiring 24, is connected to via 25. Via 25 is not connected to slot 11a. Thus, the Examiner's assertion that "first pad 12a is part of first I/O slot 11a and is therefore 'connected' to the first I/O slot," is incorrect. Accordingly, Applicants respectfully request the Examiner to withdraw this basis for rejection of claims 1, 6-8, 10, and 15-20 under 35 U.S.C. § 112, second paragraph.

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REJECTION UNDER 35 U.S.C. § 103(a)

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. (*See* M.P.E.P. § 2143.03 (8th ed. 2001)). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." (M.P.E.P. § 2143 (8th ed. 2001)).

Regarding the rejection under 35 U.S.C. § 103(a) of claims 1, 6-8, 10 and 15-20, claim 1 recites a combination including, at least, "a first pad arranged on a wiring level different from said first I/O slot and arranged above the first I/O slot without being connected to the first I/O slot."

Applicants' so-called admitted prior art (Fig. 4) discloses a first pad 12a connected to the first slot 11a. Further, with regard to Fig. 4, the specification for the present application describes at page 3, lines 3-5, that "[t]he pad 12a is connected to the I/O slot 11a [i.e., the first slot] via a wiring 14 and a via 15." Thus, Applicants' so-called admitted prior art does not teach or suggest at least a first pad "arranged above the first I/O slot without being connected to the first I/O slot," as recited in claim 1.

In contrast, and as noted above, Fig. 2 of the present application a first pad 12a is arranged above the first I/O slot 11a without being connected to the first I/O slot. Specifically, pad 12 is not arranged on the same wiring level as the first I/O slot 11a,

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and therefore not a part of first I/O slot 11a. Pad 12a connects to via 15 (through wiring 14) and further connects to via 22 (through wiring 21). Via 22 is connected to via 23 and, through wiring 24, is connected to via 25. Via 25 is not connected to slot 11a.

Janai fails to cure the deficiencies of Applicants' so-called admitted prior art. The Examiner concludes that "it would have been obvious to one of ordinary skill in the art at the time the invention to include the vertical metal strips of Janai's invention in order to customize a semiconductor device (without changing the basic wiring pattern) without increasing its general complexity." Office Action, pg. 4. The generalized statements are of questionable relevance insofar as Applicants' invention as claimed, and the Examiner does not provide any factual documentary evidence in support of this allegation of obviousness. Janai discloses a customizable three metal layer gate array device. A plurality of fusible links interconnect a plurality of transistors into an inoperable integrated circuit blank. Further, removing some of the fusible links renders the circuit blank into an operable gate array device. (*See* Abstract.) Thus, Janai relates to forming a gate array device, whereas the present application relates to making use of a pad in an integrated semiconductor circuit. (*See* page 1, lines 11-13 of the present application.) Because of this difference, Janai makes no reference to a pad. Accordingly, Janai does not disclose or suggest (nor does the Examiner allege that Janai discloses) at least a structure wherein a first pad is "arranged above the first I/O slot without being connected to the first I/O slot," as recited in claim 1.

Because a combination of Applicants' so-called admitted prior art and Janai does not teach or suggest at least the claimed first pad, the § 103(a) rejection of claim 1 should be withdrawn.

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In addition, the Examiner admits at page 3 of the Office Action that Applicants' so-called admitted prior art does not disclose the claimed "third wiring." Janai also fails to teach or suggest the claimed "third wiring." Particularly, Janai discloses vertical metal strips M2 that overlay the M1 layer (Janai, col. 2, line 58). As shown in Fig. 1A of Janai, vertical metal strips M2 are not "arranged in an outermost peripheral region of the chip," as recited in claim 1. Because a combination of Applicants' so called admitted prior art and Janai does not teach or suggest at least the claimed third wiring, the § 103(a) rejection of claim 1 should be withdrawn for this reason as well.

Additionally, by arranging the first pad "above the first I/O slot without being connected to the first I/O slot," and having a third wiring "arranged in an outermost peripheral region of the chip" and "serving to connect the other end of the first wiring to an I/O slot different from the first I/O slot," the semiconductor integrated circuit device of claim 1 enables an I/O slot requiring good characteristics (such as second I/O slot 11b, for example) to be connected to a pad having good characteristics (such as first pad 12a, for example) without changing a wiring pattern in an inner region of the chip. Thus, manufacturing costs can be reduced by using conventional masks on the chip uppermost level and the conventional built-up substrate of the package. The device of Janai does not realize these advantages of implementations of the present invention.

Further, Janai would not have motivated one of ordinary skill in the art to modify Applicants' so-called admitted prior art (Fig. 4) to result in the claimed invention, because Janai discloses fusing fusible links provided in an inner peripheral region of the chip. Particularly, Janai discloses a device including an array of semiconductor elements interconnected by fusible links. Fusing the links enables a particular function

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of the gate array device. However, before any links are fused, the circuit is inoperable. Thus, if Janai were modified so that fusible links M2 were provided only in "an outermost peripheral region of the chip," none of the semiconductor elements would be rendered operable. Accordingly, Janai provides no motivation nor any reasonable expectation of success for modifying Applicants' so-called admitted prior art to result in the claimed invention.

Because the Examiner provides insufficient evidence and reasoning as to why a skilled artisan having Applicants' so-called admitted prior art and Janai before him would have desired to make such a combination, the Examiner has not established a *prima facie* case of obviousness in rejecting claim 1 and the § 103(a) rejection of claim 1 should be withdrawn.

The § 103(a) rejection of claims 6-8, 10 and 15-20 should be withdrawn as well, at least in view of their dependence from allowable claim 1.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

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Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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